AN10714_1

Using the BLF574 in the 88-108 MHz FM band

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Document information

Info	Content
Keywords	BLF574, HV LDMOS
Abstract	This application note describes the Class-B CW (FM) performance of the 50V, unmatched, BLF574 device in the 88 – 108 MHz frequency band.

founded by Philips

Revision history

Rev	Date	Description
1.01	9 June 2008	Revision 1.01
1.02	24 July 2008	Change in Figure 3, list of components, for component B1

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1. Introduction

The BLF574 is a new, 50V, push-pull transistor using NXP's High Voltage 6th generation of LDMOS technology. The two push-pull sections of the device are completely independent from each other inside the package. There is an internally integrated ESD diode protecting the gates of the device.

The device is unmatched and is designed to be used for applications anywhere below 600 MHz where very high power and efficiency are required. Common applications would be FM and VHF broadcast, or in laser or ISM applications.

Great care has been taken during the design of the high voltage process to ensure that the device achieves high ruggedness. This is a critical parameter for successful broadcast operations. The device can achieve greater than a 10:1 VSWR for all phase angles at full operating power. Another design goal was to minimize the size of the applications circuit. This is important in that it will allow amplifier designers to maximize the power in a given amplifier size. The design highlighted in this application note achieves 600W in the 88-108 MHz band in a space smaller than 2" x 4". The circuits is only as wide as the transistor itself, so transistors can be arranged in the final amplifier as close as physically possible and still enable adequate room for the circuit implementation.

This application note describes the design and the performance of the BLF574 for Class-B CW and FM type applications in the 88-108 MHz frequency band.

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2. Circuit Diagram and Layout

2.1 Circuit Schematics

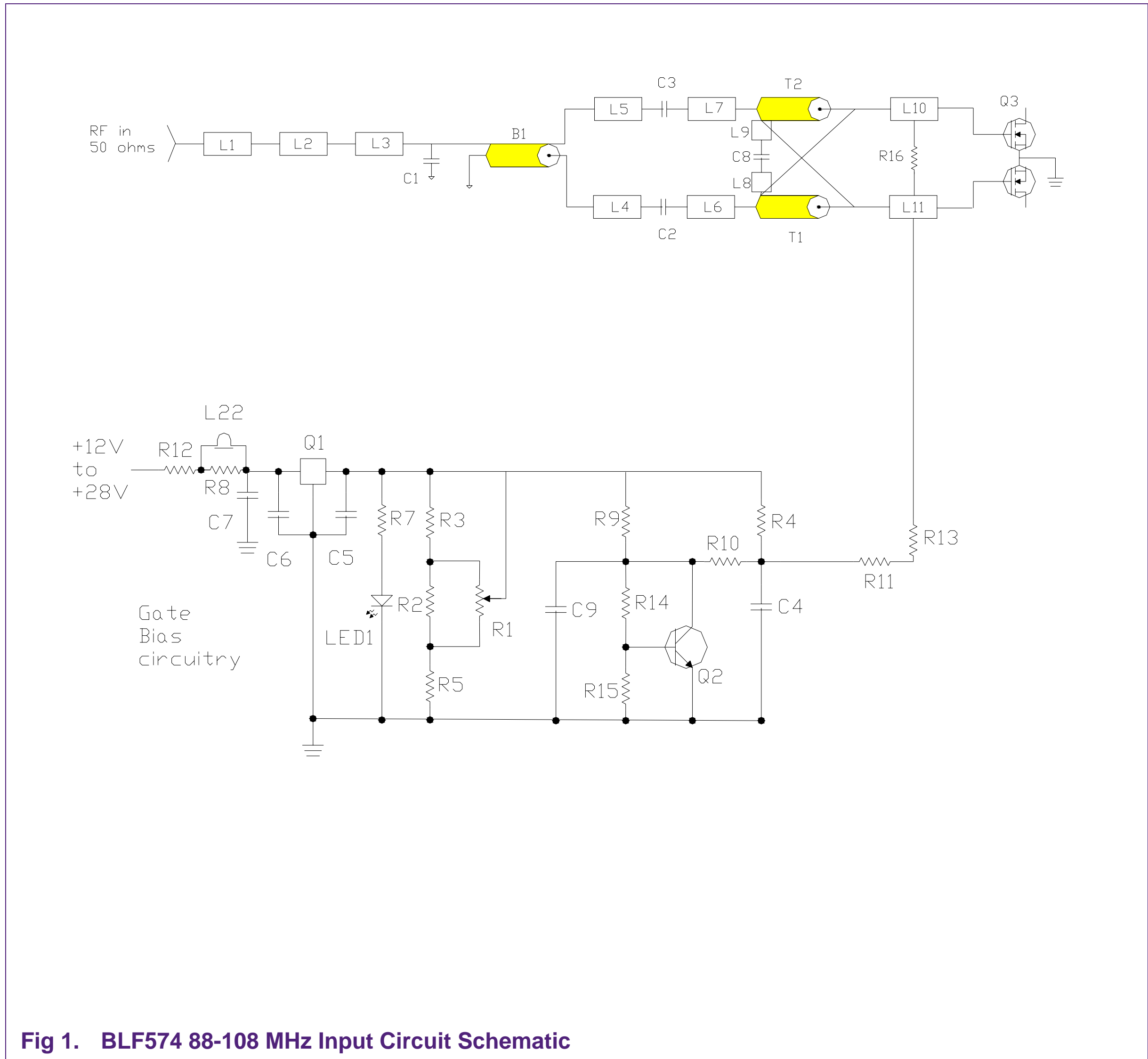

Fig 1. BLF574 88-108 MHz Input Circuit Schematic

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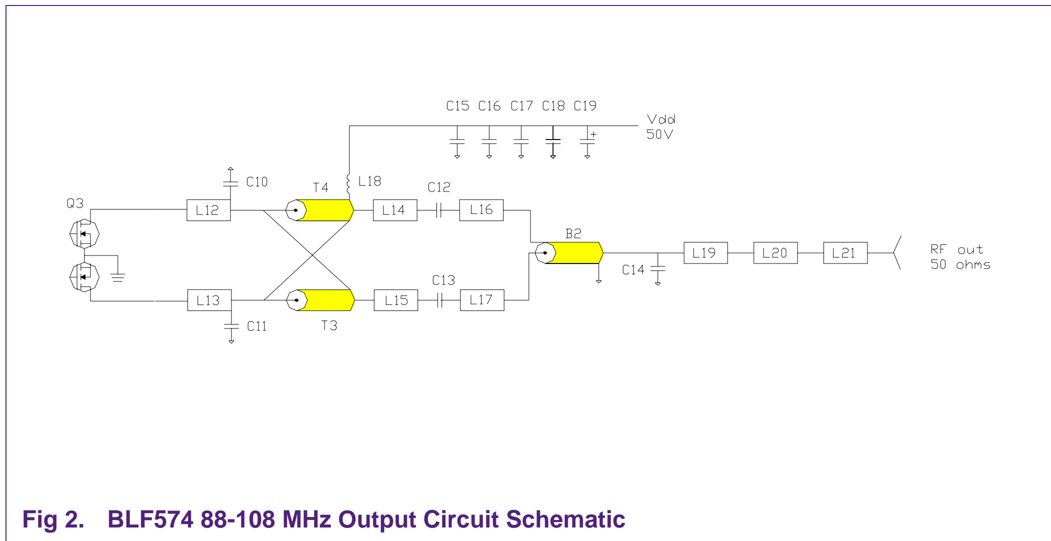

Fig 2. BLF574 88-108 MHz Output Circuit Schematic

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2.2 List of Components

List of components BLF574 Layout			
Component	**Description**	**Component**	**Description**
Q1	78L08 voltage regulator	C1, C10, C11	ATC – ATC100B220GT500X 22pF
Q2	2N2222	C2, C3	ATC – ATC700B472JT500X 4700pF
Q3	BLF574	C4, C7	Murata – GRM31MR71H105KA88L 1uF
		C5, C6, C9	Murata – GRM21BR71H104KA01L 100nF
Microstrip	Length x Width (mils)	C8	ATC – ATC100B621JT100X 620pF
L1	855 x 69	C12, C13	ATC – ATC100B301JT200X 300pF
L2	364 x 65	C14	ATC – ATC100B7R5CT500X 7.5pF
L3	390 x 69	C15	ATC – ATC100B180JT500X 18pF
L4, L5	243 x 218	C16	Murata – GRM21BR72A104K 100nF
L6, L7	See artwork file	C17	N/A
L8, L9	205 x 218	C18	Murata - GRM32ER72A225A35 2.2uF
L10, L11	511 x 520	C19	United Chemi-Con – EKMG101ELL102MM40S 1000uF
L12, L13	345 x 520		
L14, L15	348 x 150		
L16, L17	See artwork file	R1	Bourns 3214W-1-201E 200Ω potentiometer
L18	3 turns, 7” 14 gauge wire on 0.450 diameter	R2, R3	Vishay Dale - CRCW0805432RFKEA 432Ω
		R4	Vishay Dale - CRCW08052K00FKTA 2kΩ
L19	834 x 69	R5	Vishay Dale - CRCW080575R0FKTA 75Ω
L20	373 x 72	R6	N/A
L21	551 x 65	R7, R9	Vishay Dale - CRCW08051K10FKEA 1.1kΩ
L22	Small ferroxcube	R8, R13	Vishay Dale – CRCW08059R09FKEA 9.1Ω
		R10	Vishay Dale – CRCW0805 11kΩ
B1	2.5” Microcoax 047-50 through Amidon ferrite core BN-61-202	R11	Vishay Dale – CRCW08055R11FKEA 5.1Ω
		R12	Vishay Dale – CRCW2010499RFKEF 499Ω
		R14	Vishay Dale – CRCW08055K10FKTA 5.1kΩ
B2	4.9 “ 0.141” 50 ohm flexible coax cable Microcoax UT-141C-Form-F	R15	Vishay Dale – CRCW0805909RFKTA 910Ω
		R16	Vishay Dale – CRCW0805300KFKEA 300kΩ
T1, T2	2.5” Microcoax 047-25-TP through Amidon ferrite core BN-61-202	LED1	King Bright – APT2012CGCK
T3, T4	3.4” 0.086” 25 ohm Belden flexible cable		
PC-board material: Taconic RF35, ε_r = 3.5, thickness 30 mils, 1oz copper on each side			

Fig 3. BLF574 88-108 MHz List of Components

The semirigid cable lengths listed in Figure 2 are illustrated in Figure 3. They are the lengths of the semigid before trimming back the outer conductor and dielectric material.

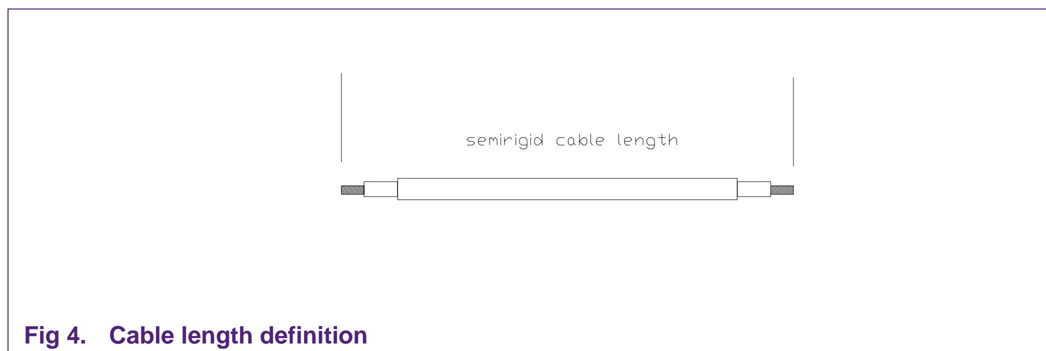

Fig 4. Cable length definition

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2.3 Layout

The following figure shows the layout of the FM band BLF574 circuit.

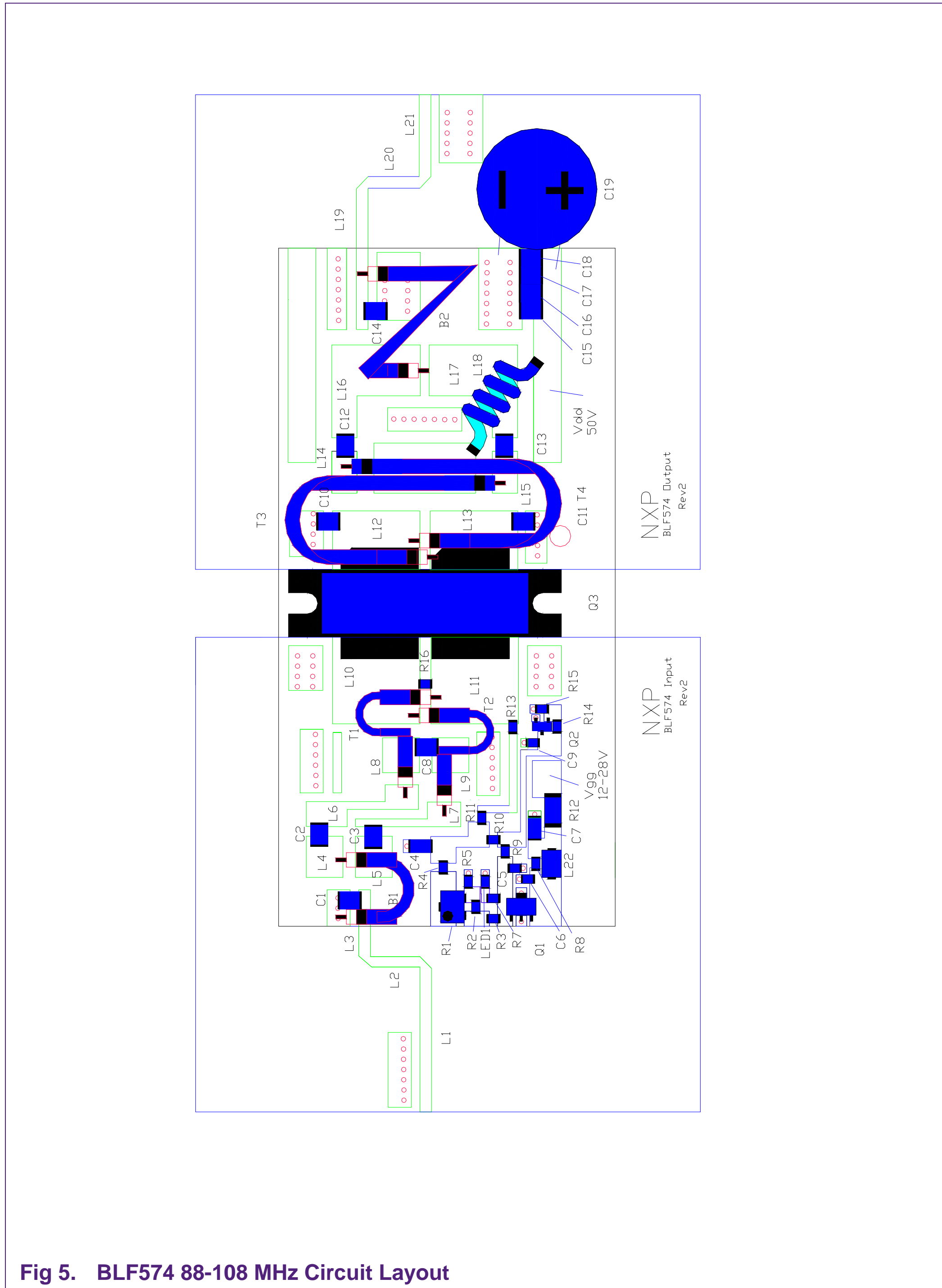

Fig 5. BLF574 88-108 MHz Circuit Layout

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2.4 Board form factor

Care has been taken to minimize board space for the design. The figure below shows how 600W can be generated in a space only as wide as the transistor itself.

Fig 6. BLF574 88-108 MHz FM demo

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3. Design of the Amplifier

3.1 Mounting Considerations

For good thermal contact, heatsink compound should be used when mounting the BLF574 in the SOT539A package to the heatsink. For an even better thermal contact, the devices can be soldered down to the heatsink. This lowers the junction temperature at high operating powers and can result in slightly better performance.

The NXP website can be consulted for application notes on the recommended mounting procedure for this type of device. Please direct your browser to

http://www.rfpower.nl/cdrom/upload/QuickUpload/File/Bolt down Recommendations.pdf

3.2 Bias Circuit

A temperature compensated bias circuit is used. The bias circuit is supplied by an 8V voltage regulator (Q1). Q2 is the temperature sensor and must be mounted in good thermal contact with the device under test, Q3. R1 sets the quiescent current. The gate voltage correction is about –4.8 to –5.0 mV/°C. R2 is used to reduce the Vgs range. Q2 generates the basic –2.2mV/°C at its base and this is multiplied up by the R14/R15 ratio for a temperature slope of about -15mV/°C. The multiplication ability of the transistor is the reason it is used rather than a diode. A portion of the –15mV/°C is summed into the potentiometer R1. R4 sets the amount of temperature compensation. The ideal value proved to be 2kΩ. The value of R11 and R13 are not important to the temperature compensation. They are used only for base band stability and to improve IMD asymmetry at lower power levels.

4. Amplifier Alignment

There are a few points within the circuit that allow performance parameters to be readily traded off for one another. In general, the following performance tradeoffs are observed when adjusting different components in the circuit:

Effect of changing output capacitor, C14:

Making the capacitor smaller than the nominal 7.5pF has the effect of improving the efficiency across the band at the expense of P1dB performance. Increasing the capacitance here will improve P1dB, but doesn't help more at the low end of the band then at the high end.

Effect of changing input capacitor, C1:

Making the capacitor smaller than the nominal 22pF has the effect of increasing the gain at the expense of P1dB.

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Effect of mounting of the output 4:1 transformers:

If the output 4:1 transformers have the middle part of the loop raised above the board, there is 0.5A or so less current draw at P1dB than if they lie flat onto the board.

Effect of lengthening the output balun:

The nominal length of the output balun is 4.9 inches. This tends to optimize performance at the high end of the frequency band. To trade in this performance to aid at the low end of the band, the balun can be lengthened from 4.9” to 8”.

Effect of adding capacitance off the drain:

The nominal capacitance off the drains is 22pF. About 0.1dB of compression performance can be gained at the expense of about 1% efficiency by taking away this capacitance. Likewise, capacitance can be added at this point to gain efficiency at the expense of linearity.

Compression performance can be traded off for higher efficiency. The two circuits use the same baseline circuit with the following differences:

Table 1. How to trade off linearity for efficiency

Component	High P1dB	High Efficiency
C12 / C13	300pF	180pF
C14	9.1pF and 3.3pF together	3.3pF
B2	8” 50 ohm	4.9” 50 ohm

The results of the two different tunes are shown in the figure below.

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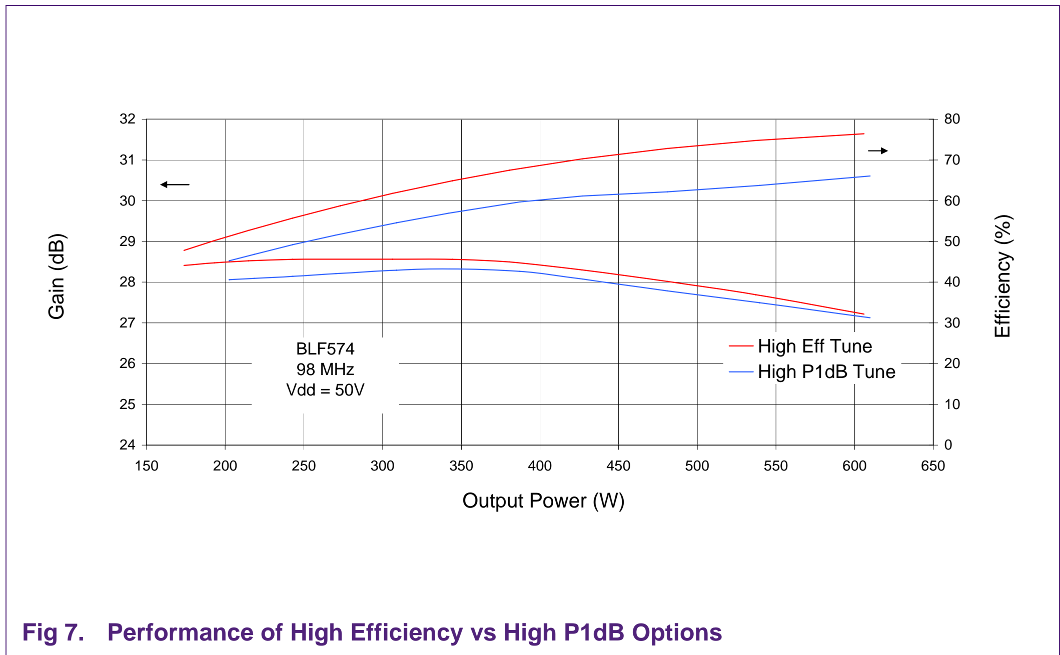

Fig 7. Performance of High Efficiency vs High P1dB Options

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5. RF Performance Characteristics

5.1 Continuous Wave Performance Summary

This table summarizes the Class-B performance of the BLF574 at 50V, 200mA, and Theatsink = 25 degrees C.

Frequency (MHz)	Output Power (W)	Gain (dB)	Efficiency (%)
88	600	27.3	71.5
98	600	27.5	75
108	600	27.5	73

5.2 Continuous Wave Performance Graphs

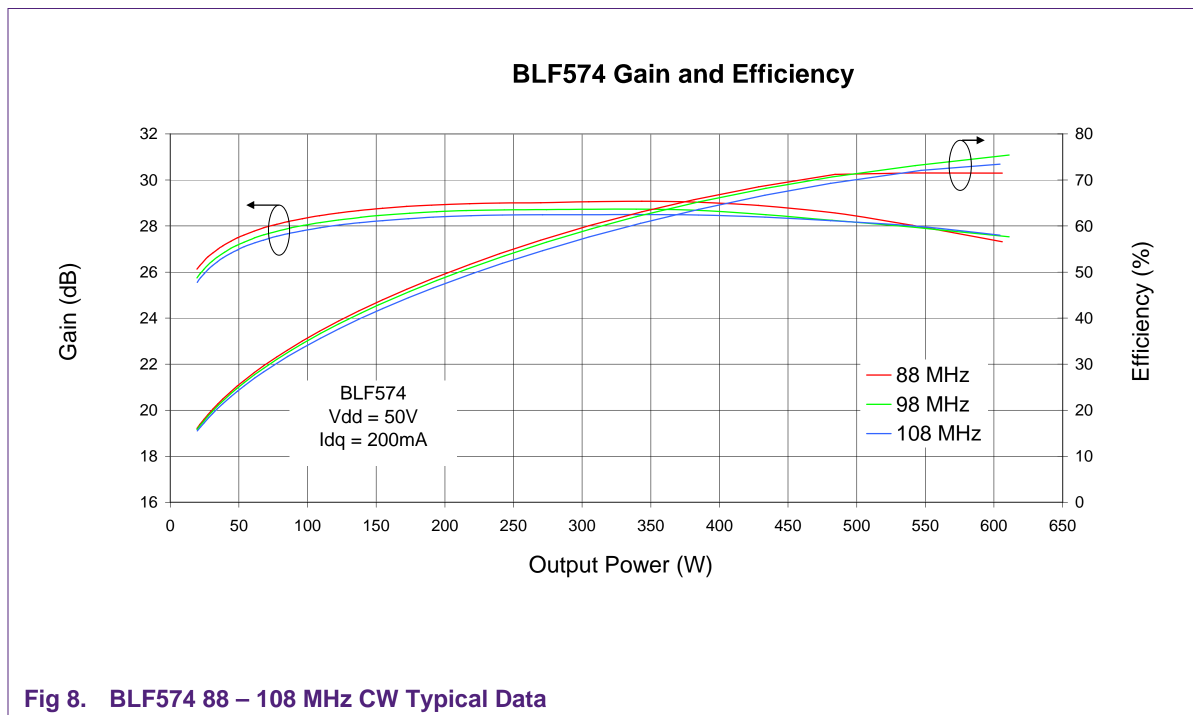

Fig 8. BLF574 88 – 108 MHz CW Typical Data

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The following figure shows how the gain and efficiency vary for a variety of drain voltage conditions.

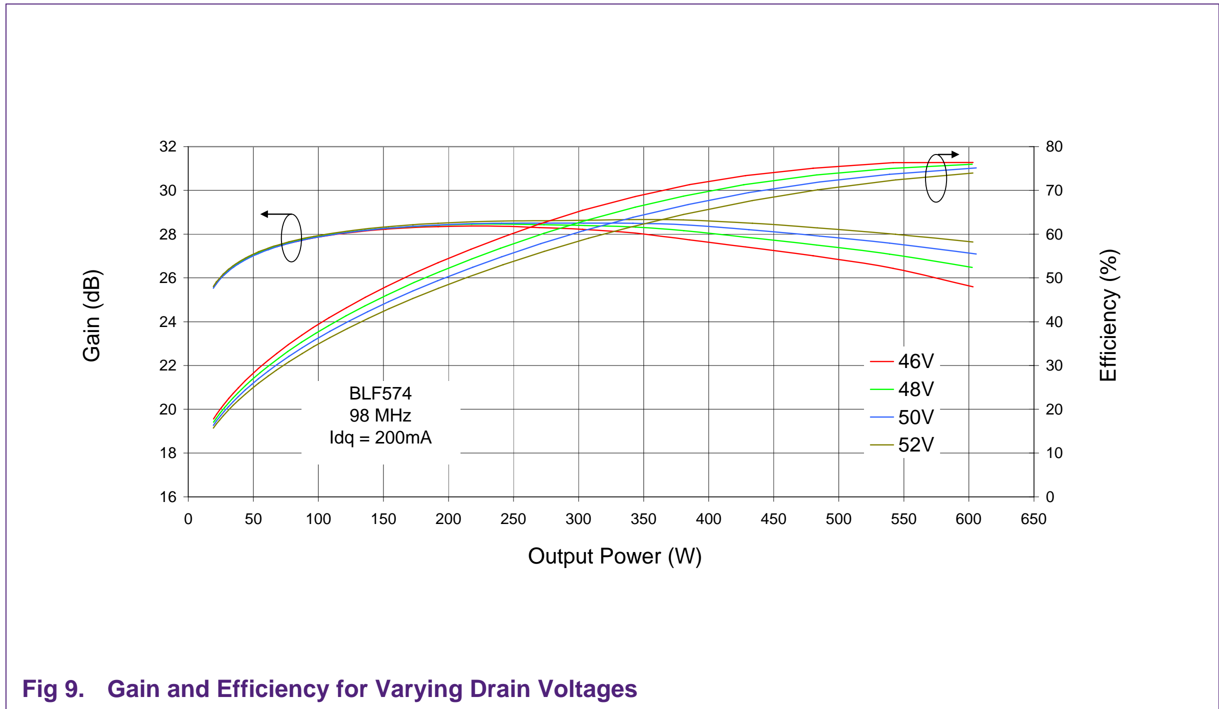

Fig 9. Gain and Efficiency for Varying Drain Voltages

Class B and Class AB performance are shown in the following figure.

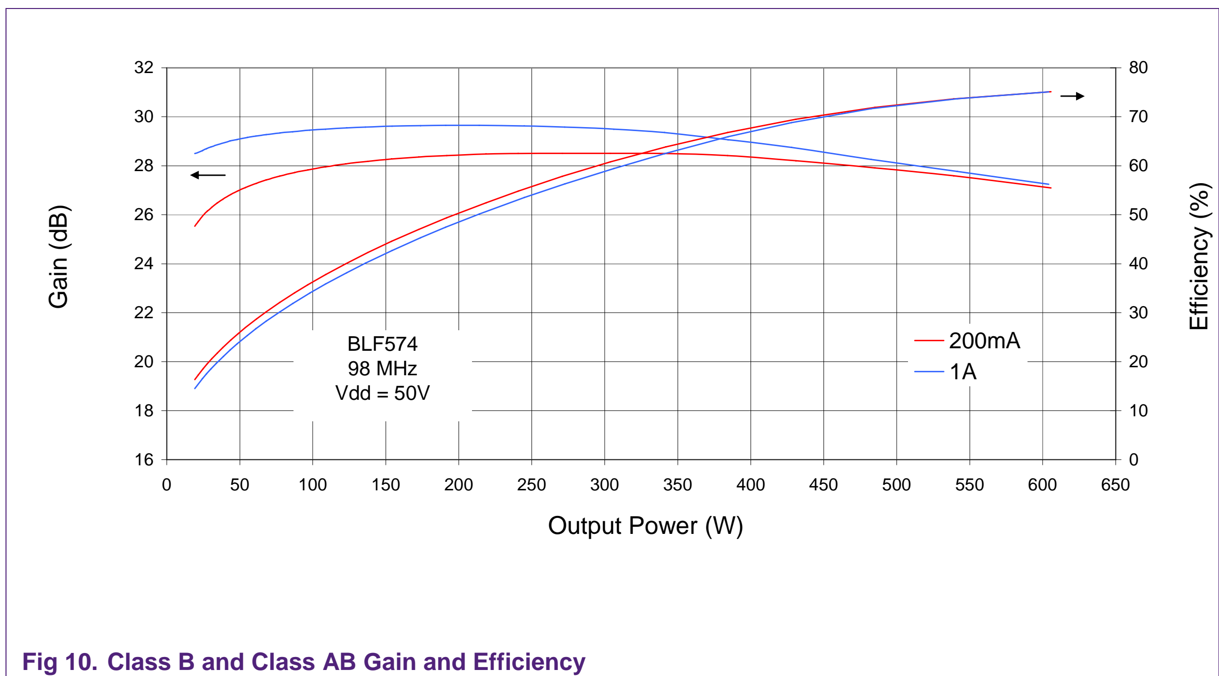

Fig 10. Class B and Class AB Gain and Efficiency

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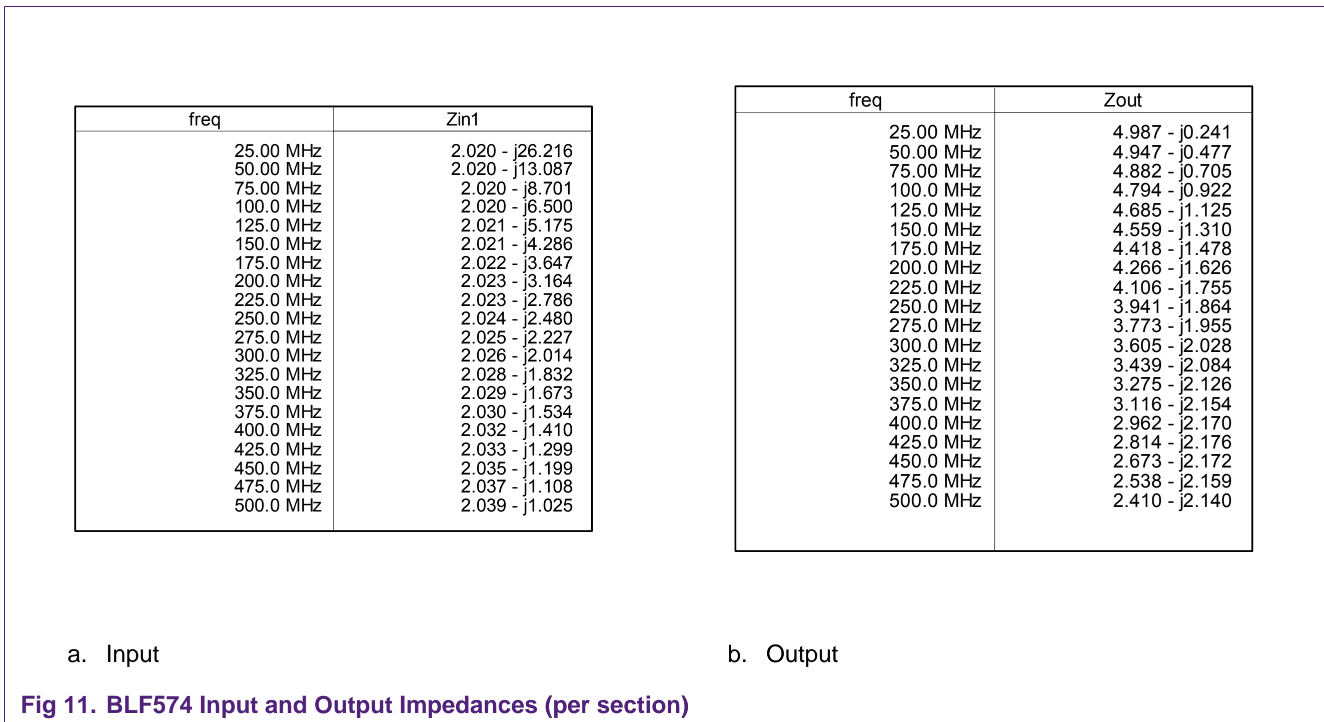
6. Impedances

The following table shows impedances for each section of the BLF574. These are generated from a first order equivalent circuit of the device and can be used to get the first pass matching circuits.



freq	Zin1
25.00 MHz	2.020 - j26.216
50.00 MHz	2.020 - j13.087
75.00 MHz	2.020 - j8.701
100.0 MHz	2.020 - j6.500
125.0 MHz	2.021 - j5.175
150.0 MHz	2.021 - j4.286
175.0 MHz	2.022 - j3.647
200.0 MHz	2.023 - j3.164
225.0 MHz	2.023 - j2.786
250.0 MHz	2.024 - j2.480
275.0 MHz	2.025 - j2.227
300.0 MHz	2.026 - j2.014
325.0 MHz	2.028 - j1.832
350.0 MHz	2.029 - j1.673
375.0 MHz	2.030 - j1.534
400.0 MHz	2.032 - j1.410
425.0 MHz	2.033 - j1.299
450.0 MHz	2.035 - j1.199
475.0 MHz	2.037 - j1.108
500.0 MHz	2.039 - j1.025

freq	Zout
25.00 MHz	4.987 - j0.241
50.00 MHz	4.947 - j0.477
75.00 MHz	4.882 - j0.705
100.0 MHz	4.794 - j0.922
125.0 MHz	4.685 - j1.125
150.0 MHz	4.559 - j1.310
175.0 MHz	4.418 - j1.478
200.0 MHz	4.266 - j1.626
225.0 MHz	4.106 - j1.755
250.0 MHz	3.941 - j1.864
275.0 MHz	3.773 - j1.955
300.0 MHz	3.605 - j2.028
325.0 MHz	3.439 - j2.084
350.0 MHz	3.275 - j2.126
375.0 MHz	3.116 - j2.154
400.0 MHz	2.962 - j2.170
425.0 MHz	2.814 - j2.176
450.0 MHz	2.673 - j2.172
475.0 MHz	2.538 - j2.159
500.0 MHz	2.410 - j2.140

a. Input

b. Output

Fig 11. BLF574 Input and Output Impedances (per section)

The convention for these impedances is shown in the figure below. They indicate the impedances looking into ½ the device.

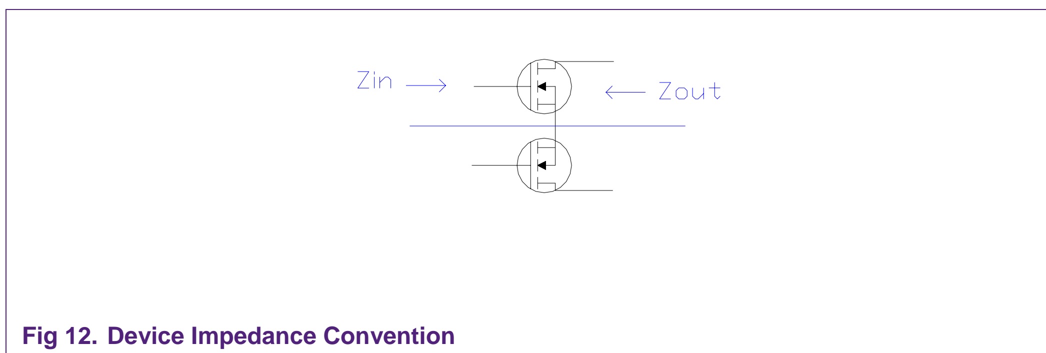


Fig 12. Device Impedance Convention

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7. Baseplate Drawings

7.1 Input Baseplate Drawing

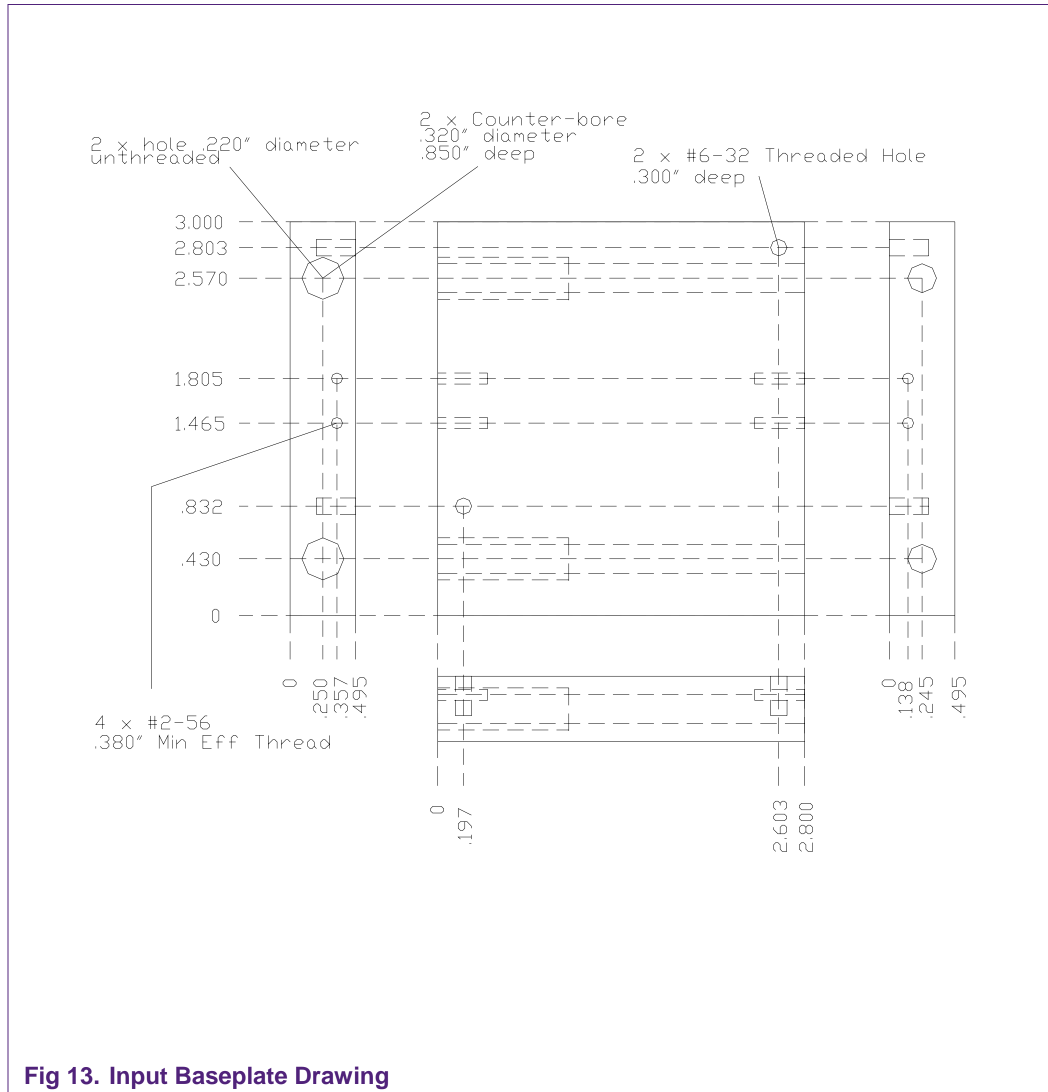

Fig 13. Input Baseplate Drawing

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7.2 Device Insert Drawing

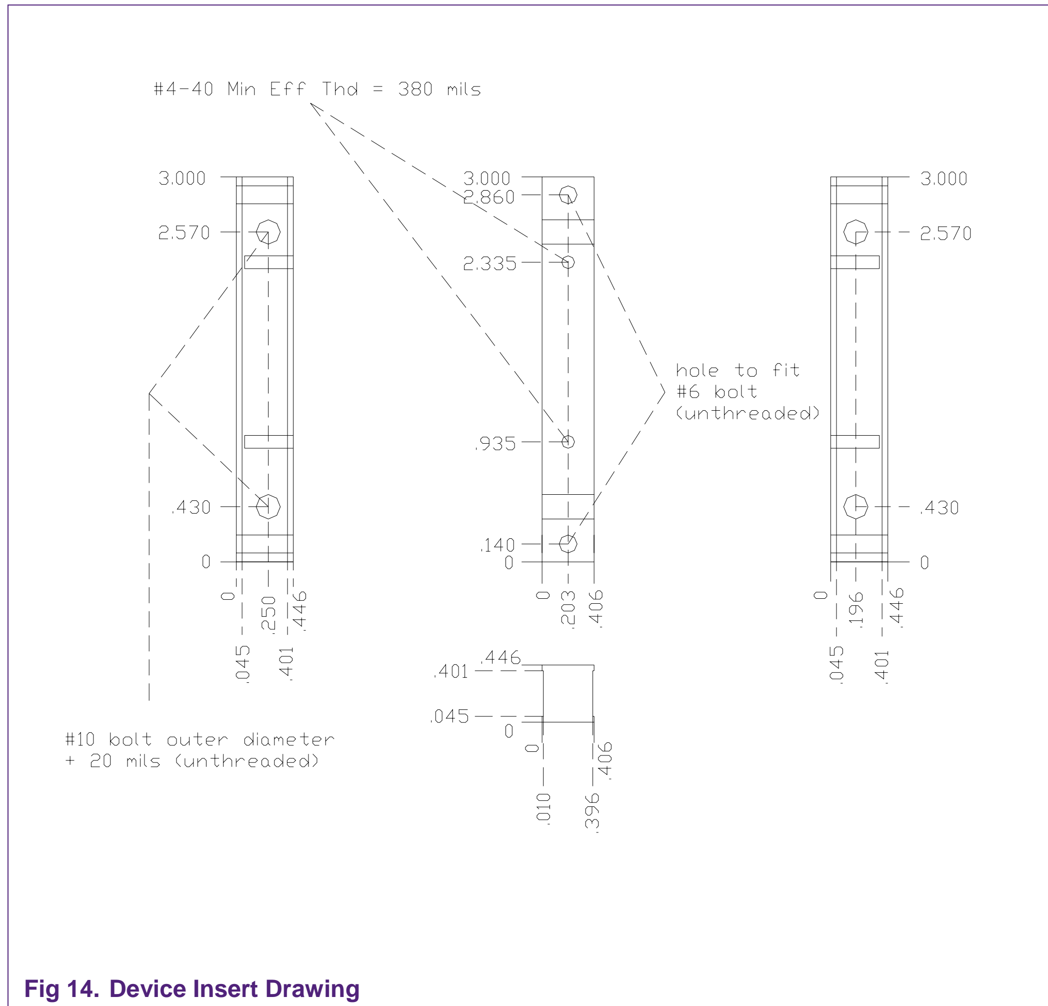

Fig 14. Device Insert Drawing

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7.3 Output Baseplate Drawing

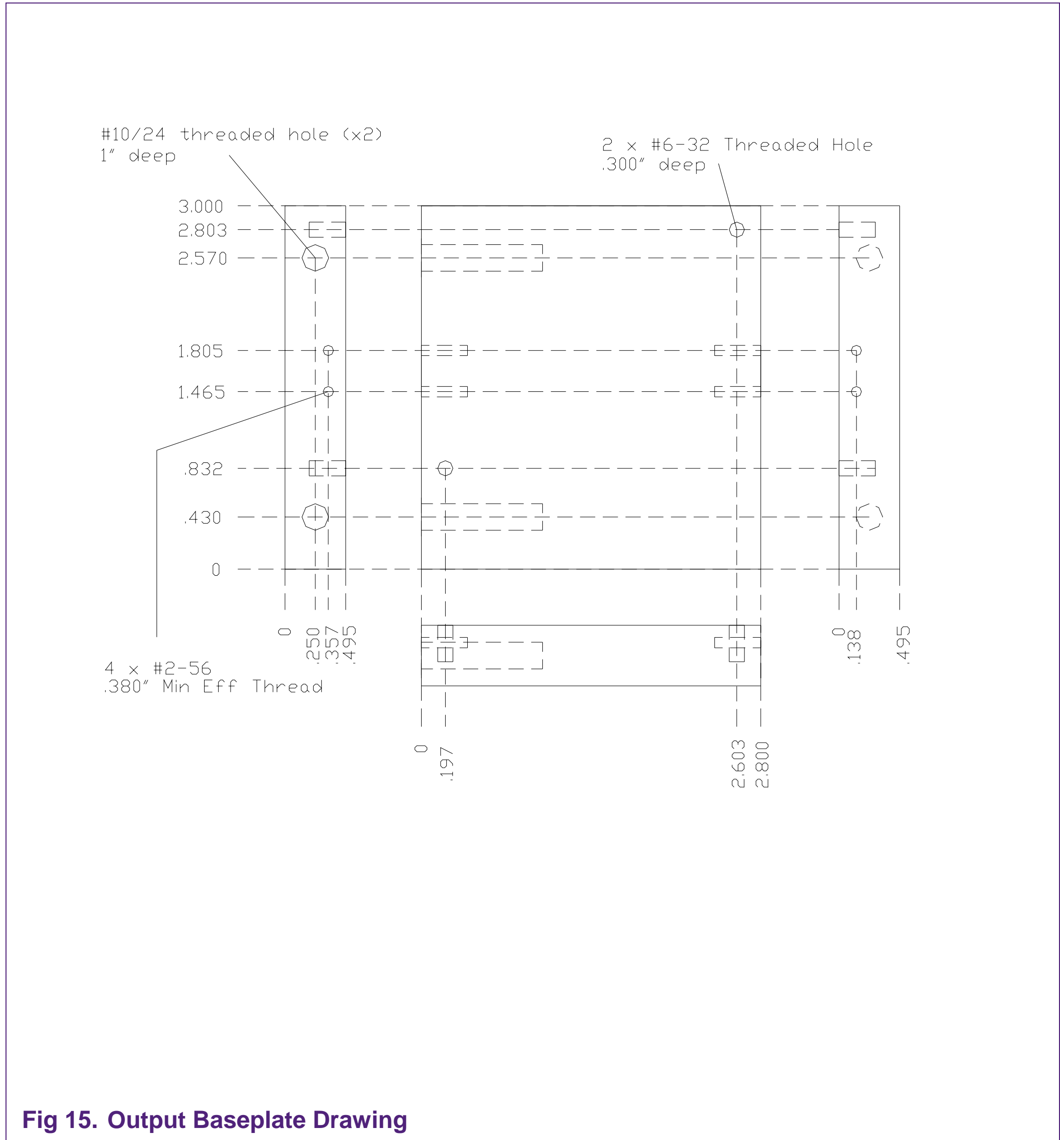

Fig 15. Output Baseplate Drawing

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8. Reliability

Time to Failure (TTF) is defined as the expected time elapsed until 0.1% of the devices of a sample size fail. The predominant failure mode for LDMOS devices is electromigration. The TTF for this mode is dependant primarily upon junction temperature, Tj. There is also a dependency upon current density. Once the device is measured, and a good knowledge is obtained for the average operating current for the application, the TTF can be calculated using the figure below.

The first step will be to use the Rth of the device to calculate the junction temperature. For the BLF574, the Rth from the junction to the device flange is 0.25 K/W. If the device is soldered down to the heatsink, this same figure can be used in determining Tj. If the device is greased down to the heatsink, the figure becomes 0.4 K/W.

From the operating efficiency, the Tj can be determined for a given heatsink temperature. For example, if the device is running at 600W of RF output power at 70% efficiency on a heatsink that is at 40 degrees C, the following TTF is calculated for a device greased down to the heatsink:

Dissipated Power = 257W

Temperature rise = Dissipated Power x Rth = 257 W x (0.4 K/W) = 103 deg C

Tj = Theatsink + Trise = 40 C + 103 C = 143 C

The operating current in this case is 17A. The curve for Tj = 140 deg C intersects the x-axis point of 17A at a TTF of 50 years. It can be estimated that 0.1% of the devices would fail in 50 years.

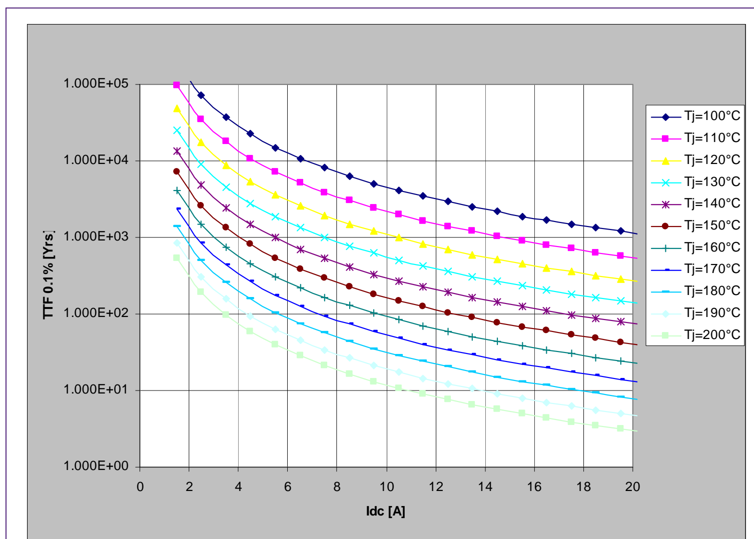

Fig 16. BLF574 Time To Failure

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9. Test Setup Block Diagram

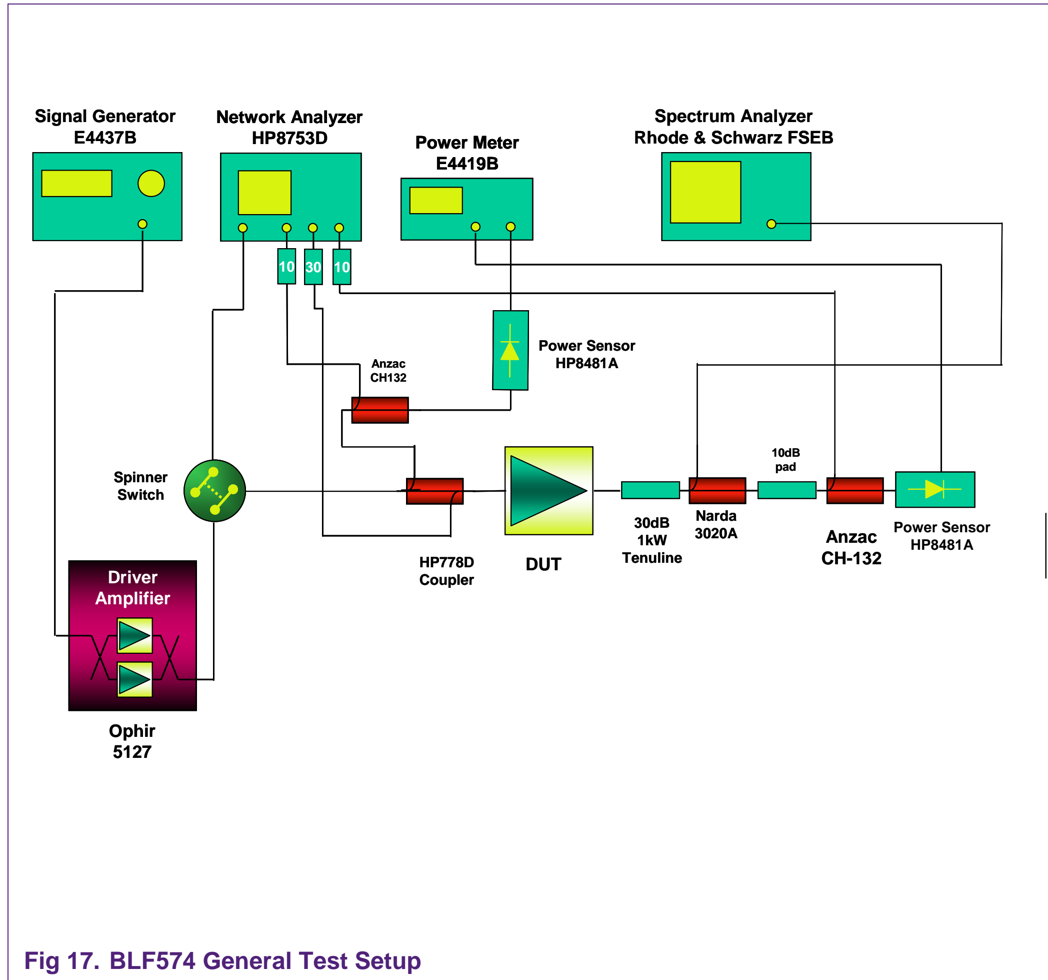

Fig 17. BLF574 General Test Setup

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10. PC Board Layout Files

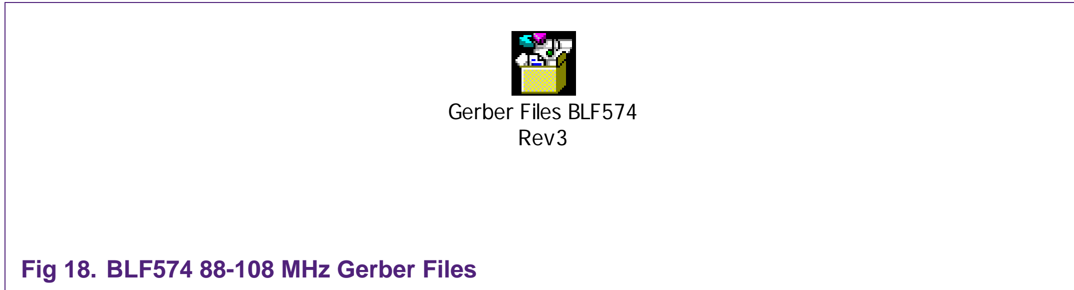

Fig 18. BLF574 88-108 MHz Gerber Files

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